RESULT CILIPADI WITH VIRTEX 6

Number of occupied Slices 368

Timing Summary:

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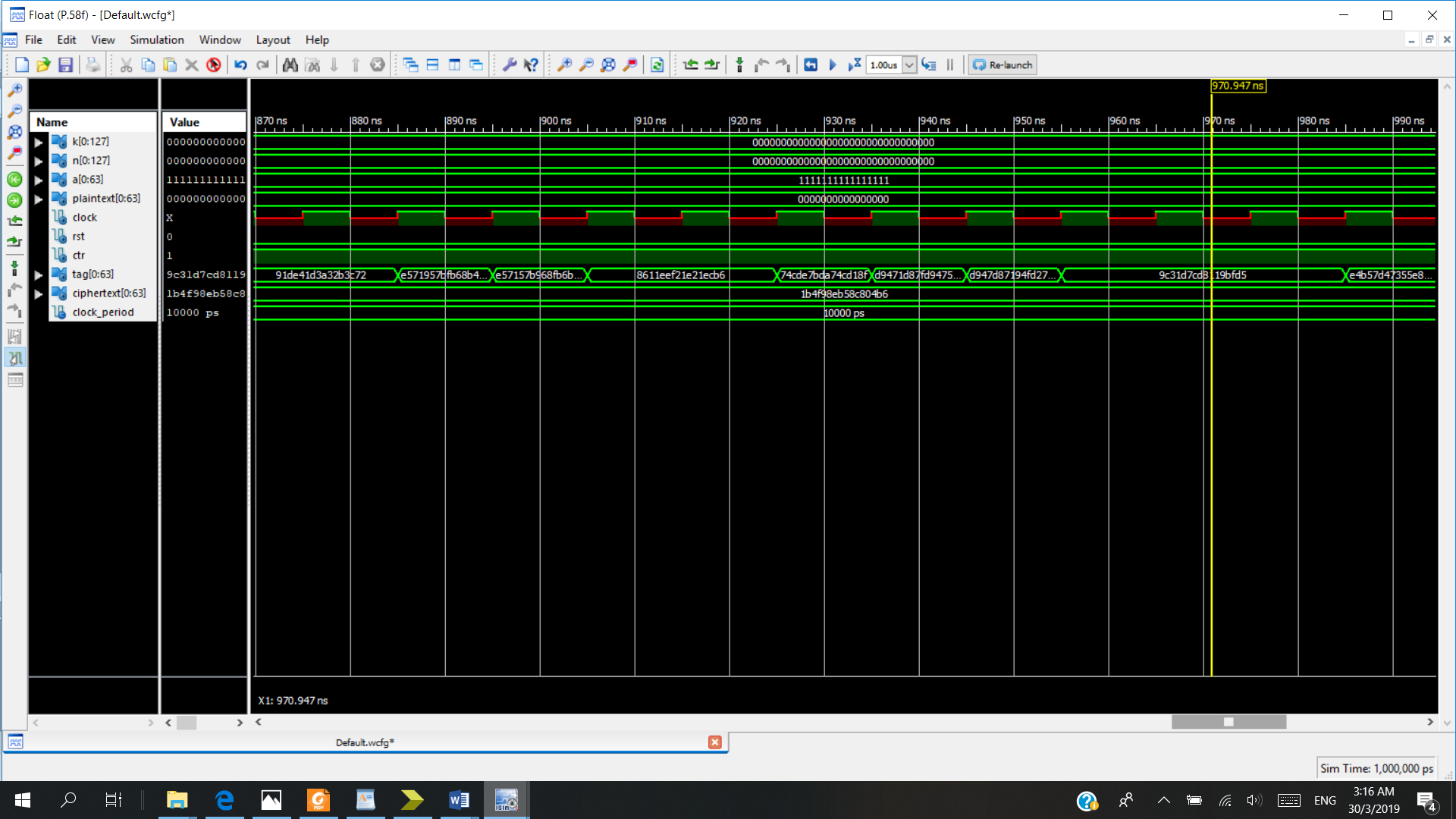
Speed Grade: -2

Minimum period: 1.563ns (Maximum Frequency: 639.959MHz)

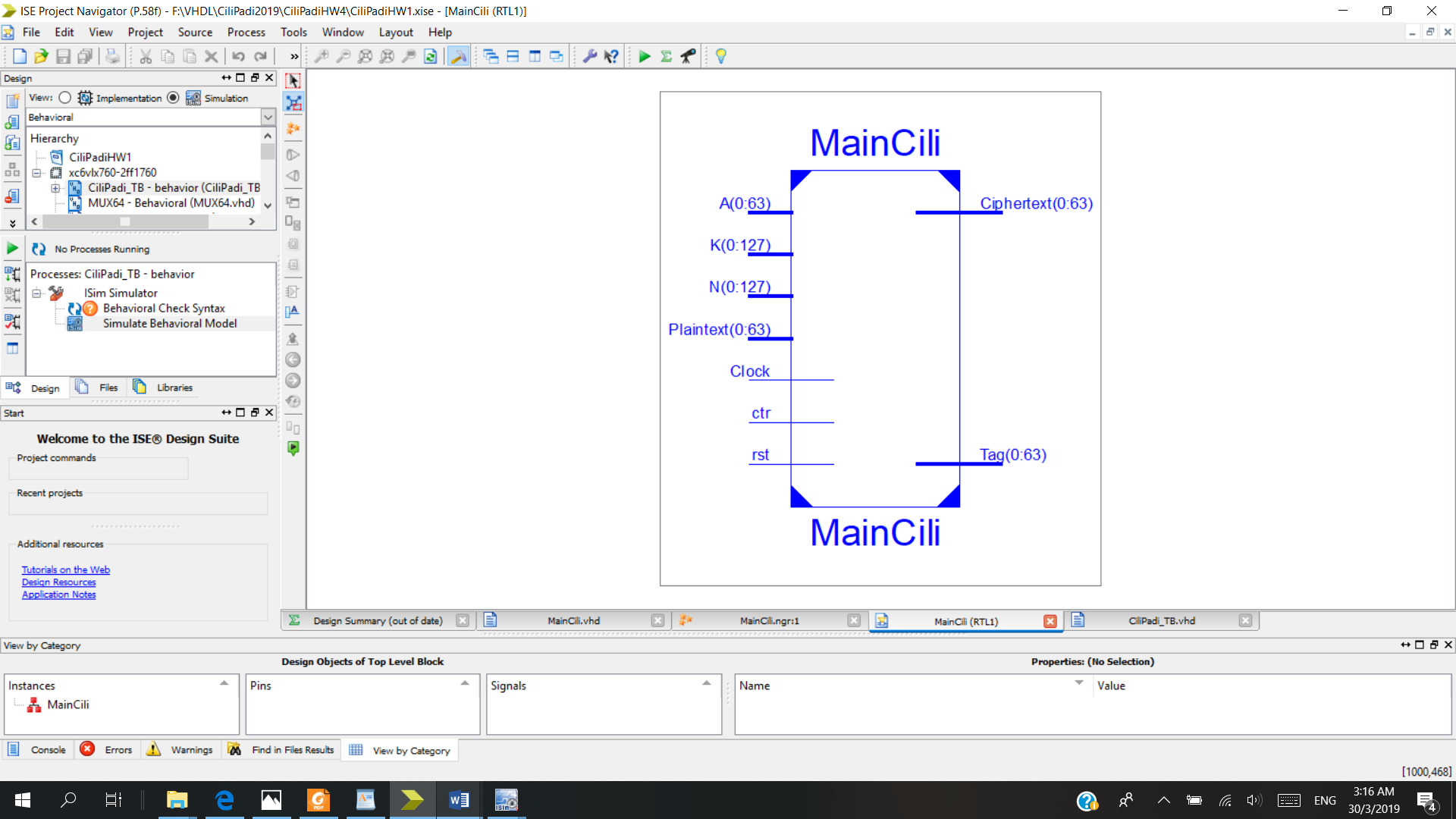
Minimum input arrival time before clock: 1.224ns

Maximum output required time after clock: 0.665ns

Maximum combinational path delay: No path found



RTL



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| **MainCili Project Status (03/30/2019 - 04:08:44)** | | | |
| **Project File:** | CiliPadiHW1.xise | **Parser Errors:** | No Errors |
| **Module Name:** | MainCili | **Implementation State:** | Placed and Routed |
| **Target Device:** | xc6vlx760-2ff1760 | * **Errors:** | No Errors |
| **Product Version:** | ISE 14.5 | * **Warnings:** | [2507 Warnings (0 new)](F://VHDL/CiliPadi2019/CiliPadiHW4/_xmsgs/*.xmsgs?&DataKey=Warning) |
| **Design Goal:** | Balanced | * **Routing Results:** | [All Signals Completely Routed](F://VHDL/CiliPadi2019/CiliPadiHW4/MainCili.unroutes) |
| **Design Strategy:** | [Xilinx Default (unlocked)](file:///C:\Users\Yasir\Desktop\Xilinx%20Default%20(unlocked)%3f&DataKey=Strategy) | * **Timing Constraints:** | [All Constraints Met](F://VHDL/CiliPadi2019/CiliPadiHW4/MainCili.ptwx?&DataKey=ConstraintsData) |
| **Environment:** | [System Settings](F://VHDL/CiliPadi2019/CiliPadiHW4/MainCili_envsettings.html) | * **Final Timing Score:** | 0  [(Timing Report)](F://VHDL/CiliPadi2019/CiliPadiHW4/MainCili.twx?&DataKey=XmlTimingReport) |

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| **Device Utilization Summary** | | | | | [**[-]**](file:///C:\Users\Yasir\Desktop\%3f&ExpandedTable=DeviceUtilizationSummary) |
| **Slice Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** | |
| Number of Slice Registers | 922 | 948,480 | 1% |  | |
| Number used as Flip Flops | 329 |  |  |  | |
| Number used as Latches | 593 |  |  |  | |
| Number used as Latch-thrus | 0 |  |  |  | |
| Number used as AND/OR logics | 0 |  |  |  | |
| Number of Slice LUTs | 624 | 474,240 | 1% |  | |
| Number used as logic | 556 | 474,240 | 1% |  | |
| Number using O6 output only | 451 |  |  |  | |
| Number using O5 output only | 0 |  |  |  | |
| Number using O5 and O6 | 105 |  |  |  | |
| Number used as ROM | 0 |  |  |  | |
| Number used as Memory | 0 | 132,480 | 0% |  | |
| Number used exclusively as route-thrus | 68 |  |  |  | |
| Number with same-slice register load | 68 |  |  |  | |
| Number with same-slice carry load | 0 |  |  |  | |
| Number with other load | 0 |  |  |  | |
| Number of occupied Slices | 303 | 118,560 | 1% |  | |
| Number of LUT Flip Flop pairs used | 1,086 |  |  |  | |
| Number with an unused Flip Flop | 232 | 1,086 | 21% |  | |
| Number with an unused LUT | 462 | 1,086 | 42% |  | |
| Number of fully used LUT-FF pairs | 392 | 1,086 | 36% |  | |
| Number of unique control sets | 13 |  |  |  | |
| Number of slice register sites lost         to control set restrictions | 14 | 948,480 | 1% |  | |
| Number of bonded [IOBs](F://VHDL/CiliPadi2019/CiliPadiHW4/MainCili_map.xrpt?&DataKey=IOBProperties) | 131 | 1,200 | 10% |  | |
| IOB Latches | 64 |  |  |  | |
| Number of RAMB36E1/FIFO36E1s | 0 | 720 | 0% |  | |
| Number of RAMB18E1/FIFO18E1s | 0 | 1,440 | 0% |  | |
| Number of BUFG/BUFGCTRLs | 11 | 32 | 34% |  | |
| Number used as BUFGs | 11 |  |  |  | |
| Number used as BUFGCTRLs | 0 |  |  |  | |
| Number of ILOGICE1/ISERDESE1s | 0 | 1,440 | 0% |  | |
| Number of OLOGICE1/OSERDESE1s | 64 | 1,440 | 4% |  | |
| Number used as OLOGICE1s | 64 |  |  |  | |
| Number used as OSERDESE1s | 0 |  |  |  | |
| Number of BSCANs | 0 | 4 | 0% |  | |
| Number of BUFHCEs | 0 | 216 | 0% |  | |
| Number of BUFIODQSs | 0 | 144 | 0% |  | |
| Number of BUFRs | 0 | 72 | 0% |  | |
| Number of CAPTUREs | 0 | 1 | 0% |  | |
| Number of DSP48E1s | 0 | 864 | 0% |  | |
| Number of EFUSE\_USRs | 0 | 1 | 0% |  | |
| Number of FRAME\_ECCs | 0 | 1 | 0% |  | |
| Number of ICAPs | 0 | 2 | 0% |  | |
| Number of IDELAYCTRLs | 0 | 36 | 0% |  | |
| Number of IODELAYE1s | 0 | 1,440 | 0% |  | |
| Number of MMCM\_ADVs | 0 | 18 | 0% |  | |
| Number of STARTUPs | 0 | 1 | 0% |  | |
| Number of SYSMONs | 0 | 1 | 0% |  | |
| Average Fanout of Non-Clock Nets | 2.57 |  |  |  | |